

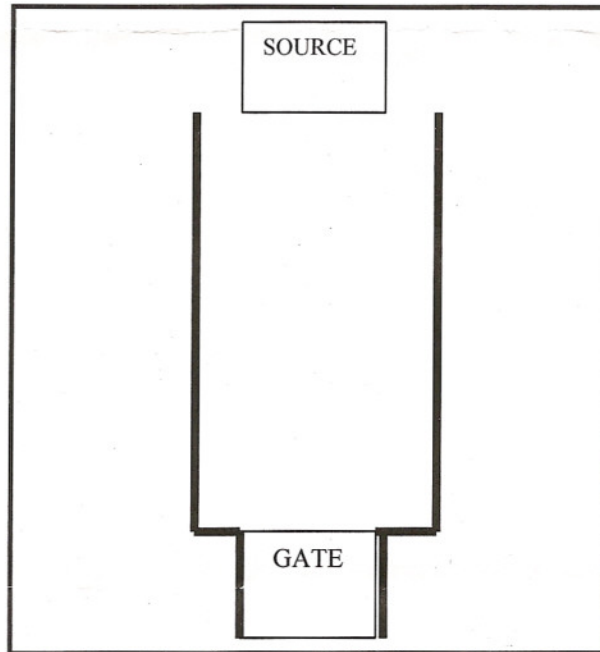


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LOGIC LEVEL HEX 1 60V N-CHANNEL GEN 3



GATE PAD: 0.020 X 0.022; SOURCE PAD: 0.023 X 0.020;

The information for this layout is believed to be correct at the time of issue. Please verify your requirements against this information, prior to commencement of any assembly process, as no liability for omission or error can be accepted.

All devices supplied against this padlayout will comply with the physical size detailed below.

Pad positions shall obey the following rules:

1. Pad functions shall not change sequence and shall agree with the above definitions.
2. No pad function shall completely change side(s) from that shown above.
3. No pad function shall move by more than 1mm from the position shown.
4. No pad function shall move from a corner, and another move into that corner, even if the above constraints are met.

<u>MANUFACTURER</u> IR	<u>APPROVAL</u> <i>Kevin Kirby</i> DATE: 1 April, 1998	<u>DIE INFORMATION</u> MAX DIMENSIONS: 0.086 X 0.076 X 0.017 MILS MANF. REF: HEX 1, 60V, N-CHAN LOGIC LV BACK POTENTIAL: DRAIN
<u>DEVICE</u> IRL014BV Gen 3	<u>SERIAL NO.</u> 001870	<u>METALISATION/THICKNESS (KA)</u> TOP: Al BACK: Cr Ni Ag